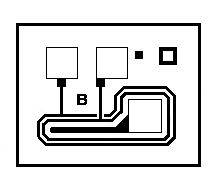
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.022”**

**.019”**

**MASK**

**REF**



**D**

**S**

**G**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0037” X .0037”**

**Backside Potential:**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .019” X .022” DATE: 12/22/16**

**MFG: SILICONIX THICKNESS .012” P/N: SD210**

**DG 10.1.2**

#### Rev B, 7/19/02